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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,036	09/09/2003	Nancy Anne Greco	YOR919950251US3 (14784AB)	2049
23389	7590	11/15/2004	EXAMINER DOLAN, JENNIFER M	
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA GARDEN CITY, NY 11530			ART UNIT 2813	
			PAPER NUMBER	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/658,036

Applicant(s)

GRECO ET AL.

Examiner

Jennifer M. Dolan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 5-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/9/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 5 is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,563,762 to Leung et al. in view of U.S. Patent No. 6,049,103 to Horikawa et al.

Leung discloses an interconnection wiring comprising: a substrate (102) having a planar upper surface of insulating and conductive regions therein (column 5, line 50 – column 6, line 47; column 7, lines 19-25); a first level of interconnection wiring (104,106) interconnecting the conductive regions; a first dielectric layer (114) formed over the first level of interconnection wiring (see figures 5 – 14), the first dielectric layer having an upper surface and having vias therein (120, 122, 220, 222) filled with a conductive material to the upper surface and in contact with regions of the first level of interconnection wiring (see figures 5 – 11; column 10, lines 57-63), at least one of the vias having dimensions to form the lower electrode of a capacitor (column 10, lines 57 – 63); a second dielectric layer (130,230) formed over the lower electrode and extending beyond the perimeter of the lower electrode (figures 9, 10, 13, 14); and a second level of interconnection wiring (134, 234) interconnecting the vias filled with conductive material (figures 10, 14) and formed over the second dielectric to form the top electrode (figures 10 and

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14). Insofar as Leung states that the bottom electrode can be formed of the filled vias (120; see column 10, lines 57-63), Leung is considered to teach all of the recited limitations. Assuming arguendo, Leung does not specifically teach or show the layout of a capacitor structure having the bottom electrode formed by filling a via.

Horikawa teaches an IC capacitor structure in which the lower electrode is alternately formed by disposing the lower electrode plate on top of a filled via (figure 1) or by disposing the lower electrode inside and completely filling a via (figures 34 – 41; column 16, lines 1 – 50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the lower electrode structure of Leung, such that the electrode is disposed in and completely fills a via, as suggested by Horikawa. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the electrode within a via, because Horikawa shows that both structures are well known in the art and used alternately for forming a capacitor, and that the structure having an electrode buried in the via has the additional advantages of reduced etching damages at the surface of the lower electrode and reduced stray capacitance (see Horikawa, column 15, lines 60-65; column 16, lines 38-50).

3. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. as modified by Horikawa et al., as applied to claim 5, supra, and further in view of U.S. Patent No. 5,920,775 to Koh.

Leung fails to specify that the bottom electrode has an upper surface of TiN and the top electrode has a lower surface of TiN.

Koh teaches that the electrodes for an IC storage capacitor are commonly formed of any of TiN, W, or stacks such as Ti/TiN/W/TiN (see column 6, lines 45-55; column 8, lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the top and bottom electrodes of Leung as modified by Horikawa is either made of TiN or a Ti/TiN/W/TiN stack, and hence have lower and upper TiN surface, as suggested by Koh. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use one of the TiN structures for each electrode, because such electrode structures are commonly used in the art, as is shown by Koh (see Koh, column 5, lines 45-55; column 8, lines 30-40) and have the advantages of acting as a diffusion barrier and having high thermal robustness, as is appreciated by one skilled in the art.

### *Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,392,189 to Fazan et al. teaches that both planar capacitor structures including a lower electrode disposed in a via and crown capacitor structures are well known in the art, analogous, and essentially interchangeable.

U.S. Patent No. 5,571,746 to Pan teaches an IC capacitor with a lower electrode formed in a via.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan  
Examiner  
Art Unit 2813

jmd

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2080